Machine Vision Development Board VDFPGA 1.0b

Developer's Guide

PRELIMINARY
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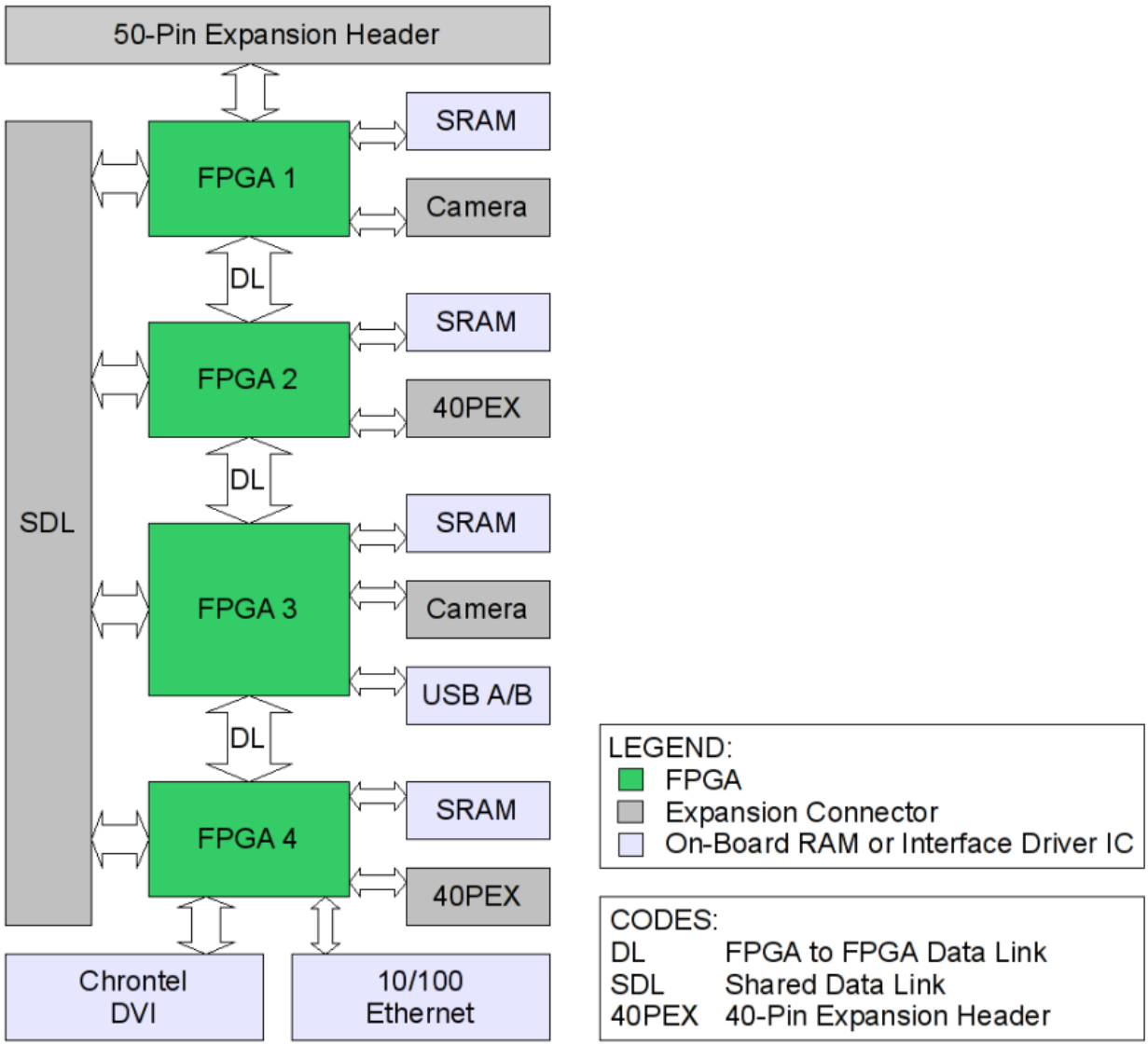
Chapter 1 Introduction to the VDFPGA

OVERVIEW

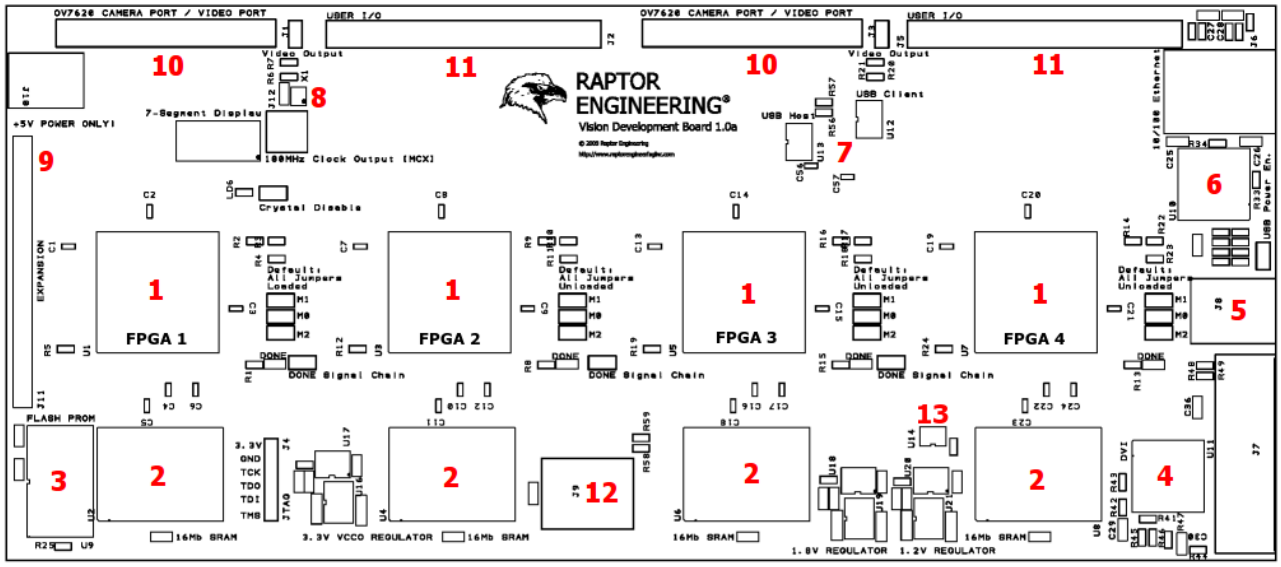
The Raptor Engineering Machine Vision Development Board [VDFPGA] is a high performance Spartan 3A-based FGPA development board, designed for demanding video processing and transmission applications. This board utilizes a fully paralleled architecture, with each of the four FPGAs having access to an independent 2MB 36-bit wide SRAM device, as well as a shared 36-bit data bus for data transmission between the four FPGAs. Additionally, one shared 25MHz clock, three dedicated inter-FPGA data links, one DVI port, one Ethernet port, two USB ports, and several expansion headers are available for use.

The majority of this document will consist of tables mapping pins on the FPGAs to respective pins on the peripheral components and expansion buses. A short troubleshooting section is available at the end of this document.

BLOCK DIAGRAM



Chapter 2 Hardware Overview



1. Xilinx Spartan 3A FPGA, XC3S1400A-FG484
2. 2MB 36-bit SRAM, Cypress CY7C1370D-200AXC
3. 32M platform flash, Xilinx XCF32P-VOG48
4. Analog/digital single-link DVI controller, Chrontel CH7301C
5. USB 2.0 function port
6. 10/100 Ethernet PHY, SMSC LAN83C185
7. 2 USB 2.0 PHY interfaces, Fairchild USB1T20
8. 25MHz clock and female MCX clock output connector, Kyocera KC3225A25.0000C30E00
9. 50-pin 2mm pitch male expansion header with 5V, 3.3V, and 1.8V power available
10. OV7620 module compatible 32-pin user I/O port with 5V power and dual I2C available
11. 40-pin 2.54mm pitch female expansion header with 5V and 3.3V power available
12. USB 2.0 host port
13. 1Kb 1-Wire secure EEPROM, Dallas Semiconductor DS2432

VDFPGA CONFIGURATION

The VDFPGA board contains several headers that allow configuration by installing shorting blocks. The following tables will assist you in configuring and connecting your VDFPGA board:

Header Name:	Action when shorted:	Action when open:
Crystal Disable	Disable crystal oscillator.	Enable crystal oscillator.
USB Power	Allow the board to be powered by the USB host that it is connected to.	Disallow USB host power.
DONE Signal Chain	Delay post-configuration enable of lower numbered FPGA until higher numbered FPGA is also configured.	Allow each FPGA to enable as soon as configuration of that particular FPGA is complete.

Header Name:	Description:
JTAG	Parallel III compatible JTAG programming header
VTO	Composite video out from nearest OV7620 camera module [if OV7620 installed]

JTAG Header Pinout

Pin Number:	Description:
1	TMS
2	TDI
3	TDO
4	TCK
5	Ground
6	+3.3V

VTO Header Pinout

Pin Number:	Description:
1	75Ω composite video output from OV7620 module
2	Ground

Chapter 3 Pinout Tables

SRAM (Identical for all FPGAs)

FPGAx Pin Number:	SRAM Pin Number:	Description:	Direction (relative to SRAM):
W3	1	DQPc	I/O
G5	2	DQC0	I/O
J5	3	DQC1	I/O
K5	6	DQC2	I/O
M5	7	DQC3	I/O
R5	8	DQC4	I/O
T5	9	DQC5	I/O
U11	12	DQC6	I/O
H5	13	DQC7	I/O
G6	18	DQD0	I/O
K4	19	DQD1	I/O
P5	22	DQD2	I/O
K6	23	DQD3	I/O
V9	24	DQD4	I/O
H6	25	DQD5	I/O
E6	28	DQD6	I/O
F7	29	DQD7	I/O
F8	30	DQPd	I/O
E7	32	A5	I
E9	33	A4	I
E10	34	A3	I
U5	35	A2	I
V14	36	A1	I
AA2	37	A0	I
AA1	43	E(36) [A19 on 4M SRAM]	I
Y2	44	A6	I
Y1	45	A7	I
W2	46	A8	I
W1	47	A9	I
V1	48	A10	I
U2	49	A11	I
U1	50	A12	I

FPGA Pin Number:	SRAM Pin Number:	Description:	Direction (relative to SRAM):
T1	51	DQPa	I/O
R2	52	DQA0	I/O
R1	53	DQA1	I/O
P2	56	DQA2	I/O
P1	24	DQA3	I/O
N1	58	DQA4	I/O
N3	59	DQA5	I/O
M1	62	DQA6	I/O
K3	63	DQA7	I/O
L1	64	SLEEP [ZZ]	I
G1	68	DQB0	I/O
F1	69	DQB1	I/O
F2	72	DQB2	I/O
E1	73	DQB3	I/O
D1	74	DQB4	I/O
D2	75	DQB5	I/O
C1	78	DQB6	I/O
C2	79	DQB7	I/O
B1	80	DQPb	I/O
E4	81	A13	I
D3	82	A14	I
F3	38	A15	I
G4	84	A16	I
H3	85	ADV/LD*	I
H2	86	OE*	I
H1	87	CEN*	I
J1	88	WE*	I
C11 + D11	89	CLK	I
K2	92	CE3*	I
J3	93	BWa*	I
K1	94	BWb*	I
N4	95	BWc*	I
P3	96	BWd*	I
T3	97	CE2	I
T4	98	CE1*	I

FPGA Pin Number:	SRAM Pin Number:	Description:	Direction (relative to SRAM):
V3	99	A17	I
V4	100	A18	I

Shared Data Link between all FPGAs

FPGA Pin Number:	Description:	Direction (relative to FPGA):
V16	User I/O	I/O
F18	User I/O	I/O
U12	User I/O	I/O
D20	User I/O	I/O
W17	User I/O	I/O
F19	User I/O	I/O
Y15	User I/O	I/O
J18	User I/O	I/O
W12	User I/O	I/O
K18	User I/O	I/O
V17	User I/O	I/O
H19	User I/O	I/O
W20	User I/O	I/O
E17	User I/O	I/O
W19	User I/O	I/O
L18	User I/O	I/O
V12	User I/O	I/O
P18	User I/O	I/O
V10	User I/O	I/O
T17	User I/O	I/O
E11	25MHz System Clock	I
G19	User I/O	I/O
E13	User I/O	I/O
N17	User I/O	I/O
E15	User I/O	I/O
K17	User I/O	I/O
V15	User I/O	I/O
R20	User I/O	I/O
U20	User I/O	I/O

FPGA Pin Number:	Description:	Direction (relative to FPGA):
N19	User I/O	I/O
V20	User I/O	I/O
N20	User I/O	I/O
R19	User I/O	I/O
T19	User I/O	I/O
N18	User I/O	I/O
T18	User I/O	I/O

FPGA1-FPGA2 Data Link

FPGA1 Pin Number:	FPGA2 Pin Number:	Description:
AB2	B2	User I/O
AA3	B3	User I/O
AB3	A3	User I/O
AA4	A4	User I/O
AB4	B4	User I/O
AB5	A5	User I/O
AA6	A6	User I/O
AB6	B6	User I/O
AB7	C5	User I/O
AA8	D6	User I/O
AB8	F13	User I/O
AB10	F15	User I/O
AB11	C7	User I/O
Y5	A7	User I/O
Y10	A8	User I/O
W6	B8	User I/O
AB12	B11	Global Clock I/O
Y6	A9	User I/O
AA12	B9	User I/O
AB13	A10	User I/O
AB14	A11	User I/O
AB15	A12	User I/O
AB16	A13	User I/O
Y9	B13	User I/O
Y12	A14	User I/O

FPGA1 Pin Number:	FPGA2 Pin Number:	Description:
Y13	A15	User I/O
W7	B15	User I/O
Y7	A16	User I/O
Y16	D8	User I/O
AB17	C8	User I/O
Y18	C12	User I/O
AB18	C14	User I/O
AB19	D16	User I/O
AA19	C16	User I/O
AB21	A19	User I/O

FPGA2-FPGA3 Data Link

FPGA2 Pin Number:	FPGA3 Pin Number:	Description:
AB2	B2	User I/O
AA3	B3	User I/O
AB3	A3	User I/O
AA4	A4	User I/O
AB4	B4	User I/O
AB5	A5	User I/O
AA6	A6	User I/O
AB6	B6	User I/O
AB7	C5	User I/O
AA8	D6	User I/O
AB8	F13	User I/O
AB10	F15	User I/O
AB11	C7	User I/O
Y5	A7	User I/O
Y10	A8	User I/O
W6	B8	User I/O
AB12	B11	Global Clock I/O
Y6	A9	User I/O
AA12	B9	User I/O
AB13	A10	User I/O
AB14	A11	User I/O

FPGA2 Pin Number:	FPGA3 Pin Number:	Description:
AB15	A12	User I/O
AB16	A13	User I/O
Y9	B13	User I/O
Y12	A14	User I/O
Y13	A15	User I/O
W7	B15	User I/O
Y7	A16	User I/O
Y16	D8	User I/O
AB17	C8	User I/O
Y18	C12	User I/O
AB18	C14	User I/O
AB19	D16	User I/O
AA19	C16	User I/O
AB21	A19	User I/O
AA21	A20	User I/O
AA22	B20	User I/O
Y21	D17	User I/O
Y22	C18	User I/O
W21	D18	User I/O
W22	C19	User I/O
V22	B17	User I/O
U21	A17	User I/O
U22	A18	User I/O

FPGA3-FPGA4 Data Link

FPGA3 Pin Number:	FPGA4 Pin Number:	Description:
AB2	B2	User I/O
AA3	B3	User I/O
AB3	A3	User I/O
AA4	A4	User I/O
AB4	B4	User I/O
AB5	A5	User I/O
AA6	A6	User I/O
AB6	B6	User I/O

FPGA3 Pin Number:	FPGA4 Pin Number:	Description:
AB7	C5	User I/O
AA8	D6	User I/O
AB8	F13	User I/O
AB10	F15	User I/O
AB11	C7	User I/O
Y5	A7	User I/O
Y10	A8	User I/O
W6	B8	User I/O
AB12	B11	Global Clock I/O
Y6	A9	User I/O
AA12	B9	User I/O
AB13	A10	User I/O
AB14	A11	User I/O
AB15	A12	User I/O
AB16	A13	User I/O
Y9	B13	User I/O
Y12	A14	User I/O
Y13	A15	User I/O
W7	B15	User I/O
Y7	A16	User I/O
Y16	D8	User I/O
AB17	C8	User I/O
Y18	C12	User I/O
AB18	C14	User I/O
AB19	D16	User I/O
AA19	C16	User I/O
AB21	A19	User I/O

OV7620 Compatible 32-Pin I/O Ports

FPGA Pin Number:	Port Pin Number:	OV7620 Description:	Direction (relative to FPGA):
B21	1	Digital output Y bus	I
B22	2	Digital output Y bus	I
C21	3	Digital output Y bus	I
C22	4	Digital output Y bus	I
D21	5	Digital output Y bus	I
D22	6	Digital output Y bus	I
E22	7	Digital output Y bus	I
E20	8	Digital output Y bus	I
F22	9	Power down mode	O
F20	10	Reset	O
G22	11	SDA [I^2C serial data]	I/O
H22	12	Frame odd field flag	I
G20	13	SCK [I^2C serial clock]	O
J22	14	Horizontal window reference	I
N/A	15	Ground	N/A
K22	16	Vertical sync	I
N/A	17	Ground	N/A
E12	18	Pixel clock	I
V11	19	External clock	O
N/A	20	+5V DC	N/A
N/A	21	Ground	N/A
N/A	22	+5V DC	N/A
M22	23	Digital output UV bus	I
L22	24	Digital output UV bus	I
N21	25	Digital output UV bus	I
N22	26	Digital output UV bus	I
P20	27	Digital output UV bus	I
P22	28	Digital output UV bus	I
R22	29	Digital output UV bus	I
R21	30	Digital output UV bus	I
N/A	31	Ground	N/A
N/A	32	Analog video output	N/A

40-Pin I/O Ports

FPGA Pin Number:	Port Pin Number:	Description:
GND	1	User I/O
+5.0V	2	User I/O
+3.3V	3	User I/O
A20	4	User I/O
B20	5	User I/O
D17	6	User I/O
C18	7	User I/O
D18	8	User I/O
B17	9	User I/O
A17	10	User I/O
A18	11	User I/O
C19	12	User I/O
B21	13	User I/O
B22	14	User I/O
C21	15	User I/O
C22	16	User I/O
D21	17	User I/O
D22	18	User I/O
E22	19	User I/O
E20	20	User I/O
F22	21	User I/O
F20	22	User I/O
G22	23	User I/O
H22	24	User I/O
G20	25	User I/O
J22	26	User I/O
K22	27	User I/O
L22	28	User I/O
M22	29	User I/O
N21	30	User I/O
N22	31	User I/O
P20	32	User I/O
P22	33	User I/O
R22	34	User I/O

FPGA Pin Number:	Port Pin Number:	Description:
R21	35	User I/O
E12	36	User I/O
V11	37	User I/O
T22	38	User I/O
U22	39	User I/O [FPGA 2 N/C]
U21	40	User I/O [FPGA 2 N/C]

50-Pin Expansion Port

FPGA Pin Number:	Port Pin Number:	Description:
B3	1	User I/O
B2	2	User I/O
A4	3	User I/O
A3	4	User I/O
A5	5	User I/O
B4	6	User I/O
B6	7	User I/O
A6	8	User I/O
D6	9	User I/O
C5	10	User I/O
F15	11	User I/O
F13	12	User I/O
A7	13	User I/O
C7	14	User I/O
Not Connected	15	Not Connected [KEY]
A8	16	User I/O
B11	17	User I/O
B8	18	User I/O
B9	19	User I/O
A9	20	User I/O
A11	21	User I/O
A10	22	User I/O
A13	23	User I/O
A12	24	User I/O
A14	25	User I/O

FPGA Pin Number:	Port Pin Number:	Description:
B13	26	User I/O
B15	27	User I/O
A15	28	User I/O
A19	29	User I/O
A16	30	User I/O
C8	31	User I/O
D8	32	User I/O
C14	33	User I/O
C12	34	User I/O
Not Connected	35	Not Connected [KEY]
D16	36	User I/O
V16	37	User I/O
A20	38	User I/O
B20	39	User I/O
D17	40	User I/O
C18	41	User I/O
D18	42	User I/O
C19	43	User I/O
B17	44	User I/O
A17	45	User I/O
A18	46	User I/O
+1.8V	47	Power
GND	48	Ground
+3.3V	49	Power
+5.0V	50	Power

Xilinx 32M PROM

The VDFGPA utilizes a single 32MB Xilinx PROM to contain all nonvolatile FPGA configuration data. This PROM will normally have some space left for user data, such as Microblaze programs. The VDFPGA has been specifically designed to allow the user to access this data, in accordance with Xilinx application note XAPP482. This feature has no effect on normal PROM programming or usage.

To accomplish this, the PROM has been permanently enabled by connecting CE to GND.
The user will need to drive CCLK [AA20] and INIT [V13], and receive data with DIN [AB20]. Because DIN is daisy-chained, the user will need to assign DOUT [AA15] to DIN [AB20] on FPGA1, 2, and 3.

For a more detailed discussion of this feature and to see Microblaze bootloader examples, please refer to the aforementioned Xilinx application note XAPP482.

Chrontel CH7301C DVI Transmitter

To enable high quality video output on modern LCD monitors and televisions, a Chrontel DVI transmitter has been installed on the VDFPGA board. This DVI transmitter features 1600x1200 maximum resolution, analog and digital output capabilities through a built-in DAC, auto-detection of connected single DVI or analog link, and optional internal conversion from the YcrCb color space to the RGB color space.

Additionally, the VDFPGA contains circuitry to utilize the standard EDID monitor information link.

For detailed specifications, please refer to the CH7301 datasheet.

FPGA Pin Number:	CH7301 Pin Number:	Description:	Direction (relative to FPGA):
AA6	63	Data input 0	O
AB6	62	Data input 1	O
AB7	61	Data input 2	O
AA8	60	Data input 3	O
AB8	59	Data input 4	O
AB10	58	Data input 5	O
AB11	55	Data input 6	O
Y5	54	Data input 7	O
Y10	53	Data input 8	O
W6	52	Data input 9	O
Y6	51	Data input 10	O
AA12	50	Data input 11	O
AB5	2	Data enable	O
AA4	48	Horizontal sync	I/O
AB4	47	Vertical sync	I/O
AA3	14	Serial port data	I/O
AB3	15	Serial port clock	O
AB13	N/A	EDID DDCDATA	I/O
AB14	N/A	EDID DDCCLOCK	O

USB 2.0 A/B Ports

The VDFPGA board includes two USB 2.0 ports—one USB A host port, and one USB B function port. A Fairchild USB1T20 transceiver is connected between each port and its host FPGA to ensure full USB 2.0 electrical compatibility.

USB A Host

FPGA3 Pin Number:	USB1T20 Pin Number:	Description:	Direction (relative to FPGA):
T22	2	HOST_OE*	O
U22	4	HOST_RX_VP	I
U21	5	HOST_RX_VM	I
W18	13	HOST_TX_VM	O
T20	12	HOST_TX_VP	O
V22	9	HOST_SPEED	O

USB B Function

FPGA3 Pin Number:	USB1T20 Pin Number:	Description:	Direction (relative to FPGA):
Y22	2	FUNCTION_OE*	O
Y21	4	FUNCTION_RX_VP	I
AA22	5	FUNCTION_RX_VM	I
W21	13	FUNCTION_TX_VM	O
W22	12	FUNCTION_TX_VP	O
AA21	9	FUNCTION_SPEED	O

FPGA4 Pin Number:	USB1T20 Pin Number:	Description:	Direction (relative to FPGA):
AB15	N/A	DPLUS_DEF_CTL	O
AB16	N/A	DMINUS_DEF_CTL	O

10/100 Ethernet PHY LAN83C185

A 10/100 Ethernet PHY has been included on the VDFPGA board to allow for fast, long-distance transmission and reception of encoded video data and/or control signals. This physical interface is designed to work with the Microblaze, the Xilinx Media Access Controller [MAC] core, and all associated software and drivers.

For detailed specifications, please refer to the LAN83C185 datasheet.

FPGA4 Pin Number:	PHY Pin Number:	Description:	Direction (relative to FPGA):
Y9	23	25MHz clock input	O
AA22	26	MDIO	I/O
Y21	27	MDC	O
Y22	29	RXD3	I
W21	30	RXD2	I
W22	31	RXD1	I
V22	32	RXD0	I
AA21	33	RX_DV	I
AB21	34	RX_CLK	I
AA19	35	RX_ER/RXD4	I
AB19	37	TX_ER/TXD4	O
AB18	38	TX_CLK	I
Y18	39	TX_EN	O
AB17	41	TXD0	O
Y16	42	TXD1	O
W7	44	TXD2	O
Y7	45	TXD3	O
Y12	47	COL	I
Y13	48	CRS	I

Dallas 1-Wire 1Kb Secure EEPROM DS2432

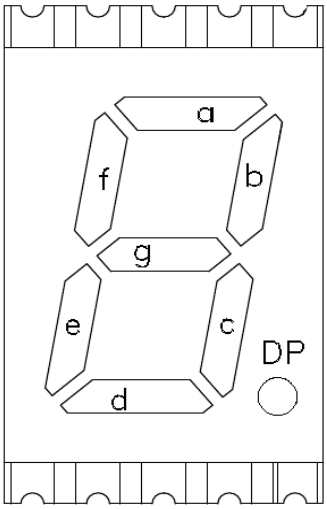
The VDFPGA incorporates, in addition to the Xilinx PROM, a user-writable 1-Wire 1Kb secure EEPROM chip with an integrated SHA-1 engine. This EEPROM is perfect for storing activation codes, network addresses, and other configuration data.

For detailed specifications, please refer to the DS2432 datasheet.

FPGA4 Pin Number:	1-Wire Pin Number:	Description:
D10	2	1-Wire

7-Segment LED and Discrete LED

One 7-segment LED display and a single discrete LED are included in the VDFPGA for simple visual debugging purposes.



FPGA1 Pin Number:	LED Pin Number:	Description:	Direction (relative to FPGA):
AA22	1	Segment E	O
Y21	2	Segment D	O
Y22	4	Segment C	O
W21	5	Dot Point	O
W22	6	Segment B	O
V22	7	Segment A	O
U21	8	Common Cathode	O
U22	9	Segment F	O
T22	10	Segment G	O
AA21	N/A	Discrete LED	O

JTAG Isolation Feature

FPGA4 can be isolated from the JTAG chain by setting FPGA4 pin AB9 low. This can be used to load immutable test/runtime designs into FPGA4 while still allowing free access to the JTAG scan chain.

Chapter 4 Selected UCF Listings

SRAM:

```
NET "SRAM_ADDR<0>" LOC = "AA2";
NET "SRAM_ADDR<1>" LOC = "V14";
NET "SRAM_ADDR<2>" LOC = "U5";
NET "SRAM_ADDR<3>" LOC = "E10";
NET "SRAM_ADDR<4>" LOC = "E9";
NET "SRAM_ADDR<5>" LOC = "E7";
NET "SRAM_ADDR<6>" LOC = "Y2";
NET "SRAM_ADDR<7>" LOC = "Y1";
NET "SRAM_ADDR<8>" LOC = "W2";
NET "SRAM_ADDR<9>" LOC = "W1";
NET "SRAM_ADDR<10>" LOC = "V1";
NET "SRAM_ADDR<11>" LOC = "U2";
NET "SRAM_ADDR<12>" LOC = "U1";
NET "SRAM_ADDR<13>" LOC = "E4";
NET "SRAM_ADDR<14>" LOC = "D3";
NET "SRAM_ADDR<15>" LOC = "F3";
NET "SRAM_ADDR<16>" LOC = "G4";
NET "SRAM_ADDR<17>" LOC = "V3";
NET "SRAM_ADDR<18>" LOC = "V4";
NET "SRAM_ADDR<19>" LOC = "AA1";
NET "SRAM_DQA<0>" LOC = "R2";
NET "SRAM_DQA<1>" LOC = "R1";
NET "SRAM_DQA<2>" LOC = "P2";
NET "SRAM_DQA<3>" LOC = "P1";
NET "SRAM_DQA<4>" LOC = "N1";
NET "SRAM_DQA<5>" LOC = "N3";
NET "SRAM_DQA<6>" LOC = "M1";
NET "SRAM_DQA<7>" LOC = "K3";
NET "SRAM_DQPA" LOC = "T1";
NET "SRAM_DQB<0>" LOC = "G1";
NET "SRAM_DQB<1>" LOC = "F1";
NET "SRAM_DQB<2>" LOC = "F2";
NET "SRAM_DQB<3>" LOC = "E1";
NET "SRAM_DQB<4>" LOC = "D1";
NET "SRAM_DQB<5>" LOC = "D2";
NET "SRAM_DQB<6>" LOC = "C1";
NET "SRAM_DQB<7>" LOC = "C2";
NET "SRAM_DQPB" LOC = "B1";
NET "SRAM_DQC<0>" LOC = "G5";
NET "SRAM_DQC<1>" LOC = "J5";
NET "SRAM_DQC<2>" LOC = "K5";
NET "SRAM_DQC<3>" LOC = "M5";
NET "SRAM_DQC<4>" LOC = "R5";
NET "SRAM_DQC<5>" LOC = "T5";
NET "SRAM_DQC<6>" LOC = "U11";
NET "SRAM_DQC<7>" LOC = "H5";
NET "SRAM_DQPC" LOC = "W3";
NET "SRAM_DQD<0>" LOC = "G6";
NET "SRAM_DQD<1>" LOC = "K4";
NET "SRAM_DQD<2>" LOC = "P5";
NET "SRAM_DQD<3>" LOC = "K6";
NET "SRAM_DQD<4>" LOC = "V9";
NET "SRAM_DQD<5>" LOC = "H6";
NET "SRAM_DQD<6>" LOC = "E6";
NET "SRAM_DQD<7>" LOC = "F7";
NET "SRAM_DQPD" LOC = "F8";
NET "SRAM_CE1_N" LOC = "T4";
NET "SRAM_CE2" LOC = "T3";
NET "SRAM_CE3_N" LOC = "K2";
NET "SRAM_OE_N" LOC = "H2";
NET "SRAM_BA_N" LOC = "J3";
NET "SRAM_BB_N" LOC = "K1";
NET "SRAM_BC_N" LOC = "N4";
NET "SRAM_BD_N" LOC = "P3";
NET "SRAM_WE_N" LOC = "J1";
NET "SRAM_CLK" LOC = "C11";
NET "SRAM_CLK_FB" LOC = "D11";
NET "SRAM_ADVLD" LOC = "H3";
NET "SRAM_SLEEP" LOC = "L1";
```

Shared Data Link:

```
NET "sharelink<0>" LOC = "V16";
NET "sharelink<1>" LOC = "F18";
NET "sharelink<2>" LOC = "U12";
NET "sharelink<3>" LOC = "D20";
NET "sharelink<4>" LOC = "W17";
NET "sharelink<5>" LOC = "F19";
NET "sharelink<6>" LOC = "Y15";
NET "sharelink<7>" LOC = "J18";
NET "sharelink<8>" LOC = "W12";
NET "sharelink<9>" LOC = "K18";
NET "sharelink<10>" LOC = "V17";
NET "sharelink<11>" LOC = "H19";
NET "sharelink<12>" LOC = "W20";
NET "sharelink<13>" LOC = "E17";
NET "sharelink<14>" LOC = "W19";
NET "sharelink<15>" LOC = "L18";
NET "sharelink<16>" LOC = "V12";
NET "sharelink<17>" LOC = "P18";
NET "sharelink<18>" LOC = "V10";
NET "sharelink<19>" LOC = "T17";
NET "sharelink<20>" LOC = "G19";
NET "sharelink<21>" LOC = "E13";
NET "sharelink<22>" LOC = "N17";
NET "sharelink<23>" LOC = "E15";
NET "sharelink<24>" LOC = "K17";
NET "sharelink<25>" LOC = "V15";
NET "sharelink<26>" LOC = "R20";
NET "sharelink<27>" LOC = "U20";
NET "sharelink<28>" LOC = "N19";
NET "sharelink<29>" LOC = "V20";
NET "sharelink<30>" LOC = "N20";
NET "sharelink<31>" LOC = "R19";
NET "sharelink<32>" LOC = "T19";
NET "sharelink<33>" LOC = "N18";
NET "sharelink<34>" LOC = "T18";
```

OV7620 Camera Port:

```
NET "camera_data_port<0>" LOC = "B21";
NET "camera_data_port<1>" LOC = "B22";
NET "camera_data_port<2>" LOC = "C21";
NET "camera_data_port<3>" LOC = "C22";
NET "camera_data_port<4>" LOC = "D21";
NET "camera_data_port<5>" LOC = "D22";
NET "camera_data_port<6>" LOC = "E22";
NET "camera_data_port<7>" LOC = "E20";
NET "camera_data_port<8>" LOC = "M22";
NET "camera_data_port<9>" LOC = "L22";
NET "camera_data_port<10>" LOC = "N21";
NET "camera_data_port<11>" LOC = "N22";
NET "camera_data_port<12>" LOC = "P20";
NET "camera_data_port<13>" LOC = "P22";
NET "camera_data_port<14>" LOC = "R22";
NET "camera_data_port<15>" LOC = "R21";
NET "camera_data_href" LOC = "J22";
NET "camera_data_pclk" LOC = "E12";
NET "camera_data_scl" LOC = "G20";
NET "camera_data_sda" LOC = "G22";
NET "camera_data_vsync" LOC = "K22";
```

25MHz System Clock:

```
NET "main_system_clk" LOC = "E11";
```

Chapter 5 Troubleshooting

Troubleshooting Guide

Problem:	Solution:
I cannot program my board—iMPACT warns that there are no devices connected.	1. Ensure that you have +5.0V connected to your board and that your JTAG cable is properly connected. 2. Try removing and reapplying power, in order to reset your board. 3. Try disconnecting and reconnecting your Parallel III programming cable at the computer (parallel port) end.
I do not have JTAG access to FPGA4 after it has been programmed!	FPGA4 will isolate itself from the JTAG scan chain if pin AB9 is driven low. Please ensure that pin AB9 is driven high if you require JTAG access to FPGA4 after a design file has been loaded.

For all other hardware problems, please contact us at support@raptorengineeringinc.com.

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Designed and manufactured in the U.S.A.
